REMARKS

Claims 1-18 are pending in the present application. Claim 16 has been amended. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Claim 16 is rejected under 35 U.S.C. 112, first and second paragraphs, as failing to comply with the written description requirement and as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More particularly, the Examiner has rejected claim 16 because of the newly added limitation, "external memory interface not operating as a data cache." Applicant has amended claim 16 to omit this limitation. No new matter as been added. Applicant, therefore, respectfully submits that claim 16 complies with 35 U.S.C. 112, first and second paragraphs.

Claims 1, 3-13 and 16-18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrel, *et al.* (U.S. Patent No. 5,829,038, hereinafter "Merrell") in view of Brabandt (U.S. Patent No. 5,809,531, hereinafter "Brabandt") and further in view of "The Cache Memory" book by Him Handy (Handy); claim 2 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel in view of Brabandt and Handy and further in view of Klein (U.S. Patent No. 6,401,199 B1, hereinafter, "Klein"); and claims 14 and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel in view of Brabandt and Handy and further in view of Stewart, *et al* .(U.S. Patent No. 5,157,780, hereinafter "Stewart"). Applicant respectfully traverses these rejections.

Claim 1 recites:

> an interface external to the internal data cache and external to the processor chip, and configured to receive cache mirror data from the processor chip, the interface further configured to discard all the cache mirror data to be written to an external

> memory received from the processor chip so that cache mirror data is never written to external memory during operation of the processor chip.

The Office Action, states:

> Merrel does not teach that all the cache mirror data to be written to an external memory received from the processor chip is never written, however Brabandt discloses the ability to have a system where no external memory is needed and therefore no writes to the external memory will ever be needed and therefore never written.

(Final Office Action, page 4.) Brabandt, however, explicitly states, "[I]t is an object of the present invention to provide a microprocessor with an on-chip cache *with no dependency upon external RAM subsystem during power-up*." (Brabandt, column 2, lines 24-27.) Brabandt, therefore, teaches away from the limitation of "an interface external to the internal data cache and external to the processor chip, and configured to receive cache mirror data from the processor chip," and cannot be combined with Merrel. Furthermore, Handy does not teach or suggest this limitation.

Even if Brabandt were assumed to be combinable with Merrel, the Office Action appears to suggest that a portion (L2-Ln) of the internal data cache of Merrel be split from L1 and located externally according to the teaching of Handy. (See Office Action, page 4.) As is alleged by the Examiner, L1 corresponds to the internal data cache and L2-Ln is the interface of claim 1. (See Office Action, page 4.) The Office Action, however, does not clearly state which piece of prior art teaches discarding all cache mirror data to be written to an external memory. While the Examiner states that external memory is unnecessary according to Brabandt, the Examiner also states at page 4 that Brabandt teaches not writing to external memory even during an eviction or flushing. Brabandt, in fact, does not teach discarding cache mirror data to be written to an external memory. Applicant, therefore, respectfully submits that claim 1 is patentable over the prior art of record.

Claims 2, 3 and 5-7 depend from claim 1 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 4 recites:

> A method of operating a processing chip having a processor, an internal data cache and a cache controller for transmitting cache mirror data write instructions out of the processing chip, the method including discarding the write instructions at an interface external to the processing chip so that cache mirror data is never written to external memory during operation of the processing chip.

The Office Action states,

> Merrel does not teach that all the cache mirror data to be written to an external memory received from the processor chip is never written, however Brabant discloses the ability to have a system where no external memory is needed and therefore no writes to that external memory will ever be needed and therefore never written.

(Office Action, page 6.) Brabandt, however, explicitly states, "[I]t is an object of the present invention to provide a microprocessor with an on-chip cache *with no dependency upon external RAM subsystem during power-up*." (Brabandt, column 2, lines 24-27.) Brabandt, therefore, teaches away from the limitation of an internal data cache and a cache controller for transmitting cache mirror data write instructions out of the processing chip. As discussed with respect to claim 1, hereinabove, even if Brabandt could be combined with Merrel, Brabandt does not teach or suggest teach discarding cache mirror data to be written to an external memory, and, therefore, cannot teach or suggest discarding the write instructions at an interface external to the processing chip. Furthermore, Handy does not teach or suggest this limitation. Applicant, therefore, respectfully submits that claim 4 is patentable over the prior art of record.

Claim 8 recites:

> an interface external to the internal data cache and external to the processor chip, the interface coupled between the processor chip and the external memory and providing the only connection between the processor chip and the address decoder, the interface configured to receive memory data from the external memory and transfer the memory data to the processor chip, the interface further configured to receive internal data cache mirror data from the processor chip and discard all the internal data cache mirror data to be written to the external memory so that the internal data cache mirror data is never written to external memory.

The Office Action states,

> Merrel does not teach that all the cache mirror data to be written to an external memory received form the processor chip is never written, however Brabandt discloses the ability to have a system where no external memory is needed and therefore no writes to that external memory will ever be needed and therefore never written.

(Office Action, page 9.) Brabandt, however, explicitly states, "[I]t is an object of the present invention to provide a microprocessor with an on-chip cache *with no dependency upon external RAM subsystem during power-up*." (Brabandt, column 2, lines 24-27.) Brabandt, therefore, teaches away from the limitations of "an interface external to the internal data cache and external to the processor chip … the interface further configured to receive cache mirror data from the processor chip," and cannot be combined with Merrel. As discussed with respect to claim 1, hereinabove, even if Brabandt could be combined with Merrel, Brabandt does not teach or suggest teach discarding cache mirror data to be written to an external memory, and, therefore, cannot teach or suggest discard all the internal data cache mirror data to be written to the external memory so that the internal data cache mirror data is never written to external memory. Furthermore, Handy does not teach or suggest this limitation. Applicant, therefore, respectfully submits that claim 8 is patentable over the prior art of record.

Claims 9-15 depend from claim 8 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Claim 16 has been amended to recite:

> transmitting cache mirror data write instructions from a first cache controller of a first integrated circuit to an external memory interface, wherein the external memory interface is located outside the first integrated circuit; and discarding the first cache mirror data write instructions at the external memory interface so that cache mirror data is never written to external memory during operation of the first processor.

The Office Action states,

> Merrel does not teach that all the cache mirror data to be written to an external memory received form the processor chip is never written, however Brabandt discloses the ability to have a system where no external memory is needed and therefore no writes to that external memory will ever be needed and therefore never written.

(Office Action, page 9.) Brabandt, however, explicitly states, "[I]t is an object of the present invention to provide a microprocessor with an on-chip cache *with no dependency upon external RAM subsystem during power-up*." (Brabandt, column 2, lines 24-27.) Brabandt, therefore, teaches away from the limitations of "transmitting cache mirror data write instructions from a first cache controller of a first integrated circuit to an external memory interface, wherein the external memory interface is located outside the first integrated circuit." As discussed with respect to claim 1, hereinabove, even if Brabandt could be combined with Merrel, Brabandt does not teach or suggest teach discarding cache mirror data to be written to an external memory, and, therefore, cannot teach or suggest discarding the first cache mirror data write instructions at the external memory interface. Furthermore, Handy does not teach or suggest this limitation. Applicant, therefore, respectfully submits that claim 16 is patentable over the prior art of record.

Claims 17 and 18 depend from claim 16 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Benjamin E. Nise, Applicant's attorney, at 972-732-1001, so that such issues may be resolved as expeditiously as possible. The Commissioner is hereby authorized to charge any fees that are due, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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